Front-end Electronics for Silicon Trackers readout in Deep Sub-Micron CMOS Technology The case of Silicon strips at the ILC.

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Abstract

For the years to come, Silicon strips detectors will be read using the smallest available integrated technologies for room, transparency, and power considerations. CMOS, Bipolar-CMOS and Silicon-Germanium are presently offered in deep-submicron (250 down to 90nm) at affordable cost through worldwide integrated circuits multiproject centers. As an example, a 180nm CMOS readout prototype chip has been designed and tested, and gave satisfactory results in terms of noise and power. Beam tests are under work, and prospectives in 130nm will be presented.

I. Context of the Silicon Strips at the ILC

A few millions of 10 to 60 cm long Silicon strips are foreseen for a large Silicon tracker at the ILC. Their thickness will be between 200 and 500µm, with a strip pitch between 50 and 200 µm. They will be single sided. DC versus AC coupling is presently being evaluated in terms of costs, and overall complexity.

A. Detector and Readout Parameters

Such Silicon strips exhibit a dominating interstrip capacitance of the order of 1 pF/cm and strip to substrate capacitance of 0.1 pF/cm. The occupancy at the ILC defined as the percentage of channels hit per beam crossing will be less than 1 % in the barrel layers, of the order of a few per cents in the end caps layers. The ILC machine will produce trains of 3000 or 6000 bunches spaced by 150 or 300 ns for 1ms, followed by an idle stage of 100 ms. During trains, data will be recorded in analogue pipe-lines, then digitised and processed during the idle stage.

B. Detector data

Both pulse height and time will be recorded. A resolution transverse to the strip of a few micrometers can be achieved using centroids, and two shaping times will be implemented, one from 500ns to 1 µs on all layers, depending mainly on strip length for beam crossing tagging, and 10-30 ns for some nanosecond timing layers intended to provide a crude measurement of the impact along the strip with a resolution of a few centimeters.

C. Coordinate along the strip

Pulse propagation evaluation along the strip using a Spice based linear model and laser diode stimulation measurement show that a current pulse induced in a strips at a given length propagates a voltage step along the strip as in a RLC transmission line with a velocity $1/\sqrt{LC}$ of the order of c / 3.7 (~ 8cm/ns), where L and C are the inductance and capacitance of the strip per unit length. The Spice model includes both strip to substrate and the interstrip capacitances as shown on Figures 1 and 2. Figure 3 shows the measured propagation when strips are illuminated with a laser diode light moved along the detector.

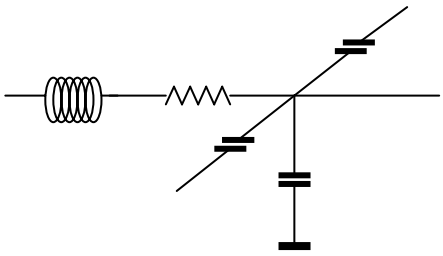

Figure 1. Strip linear model

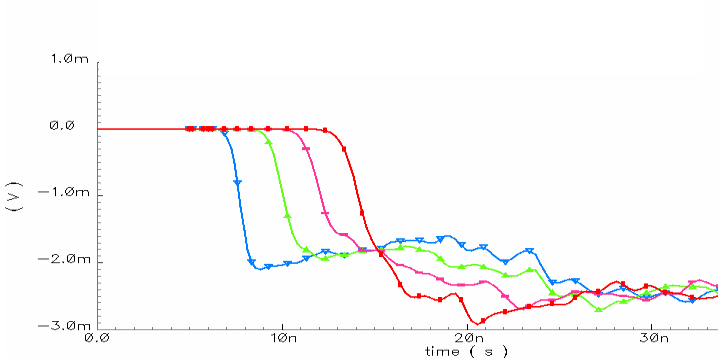

Figure 2. Spice simulation of a propagating voltage pulse along a microstrip detector.

Work in the framework of the SiLC R&D (Silicon for the Linear Collider) collaboration and the EUDET I3-FP6 European project

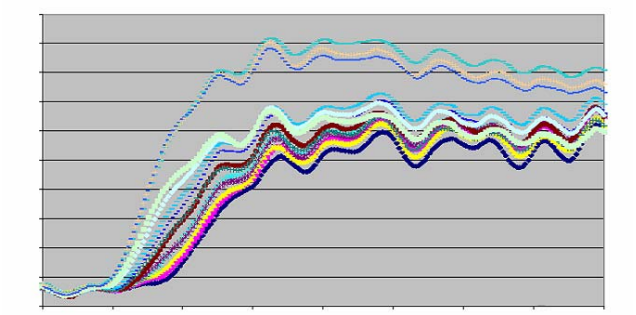

Figure 3. Measured relative response moving a laser light source by 0 to 24 cm along the strip (horizontal scale 50 ns).

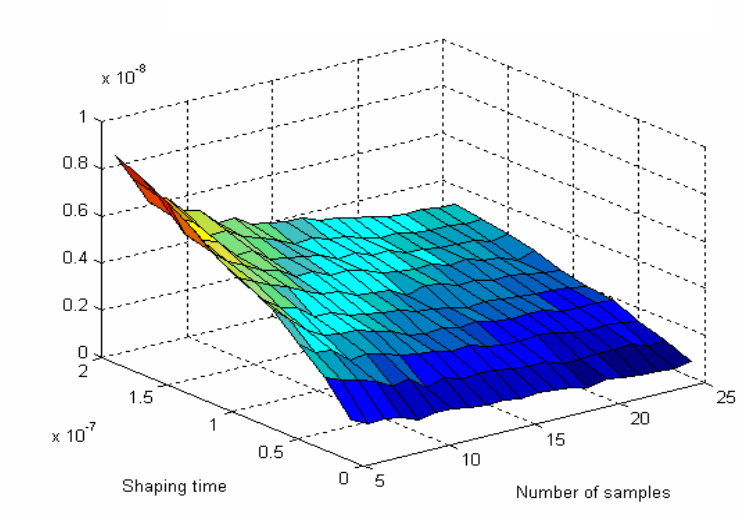

Figure 4. Simulated time resolution as a function of the shaping time, and the number of samples. Signal to noise is set to 25. Least square time estimation using the Cleland and Stern algorithm Ref[1].

II. TECHNOLOGIES

The Silicon detector and VLSI technologies allow today to improve both detector and front-end integration. Front-end chips implemented in deep sub-micron CMOS technologies down to 90nm allow to integrate hundreds if not thousands of channels at a reduced power budget, thanks to the reduction of all wiring capacitors. Silicon-Germanium exhibits less 1/f noise for a bandwidth improved by one order of magnitude, chip thinning, bump bonding and even 3D integration Ref[2]. will allow smaller pitch detectors and consequently better position and time resolution, for less on-detector material.

III. INTEGRATED FRONT-END ELECTRONICS

The data sketched above can be obtained from the detector with pulse sampling allowing to get accurate amplitude and timing. Sparsification is to be performed in the front-end, using thresholds on analogue sums of adjacent channels. Calibration can also be integrated in the front-end chips using Digital to Analogue Converter and Metal Insulator Metal capacitors of known values as charge reference, together with switches networks.

During data taking, activity exceeding the threshold on a given channel will be stored in a 16-deep analogue pipe-line including pedestal, and digitised after the train in parallel for all channels with a 10-bit Wilkinson Analogue to Digital Converter. In case a strip is hit several times during a train, an event buffer can record 16 sets of samples. The analogue pipe-line has therefore two dimensions, along time and events.

Digital signal processing in the front-end can perform some low level tasks such as centroids, least squares amplitude and time fits, lossless data compression, error correcting codes.

Power will be carefully optimised, taking into account the duty cycle of the ILC machine allowing to save at more a factor of 100. On the ILC detector, the voltages supplies will be ramped in a round robin scheme to avoid high current spikes on single spots in the detector.

The foreseen front-end chip architecture is depicted on Figure 5.

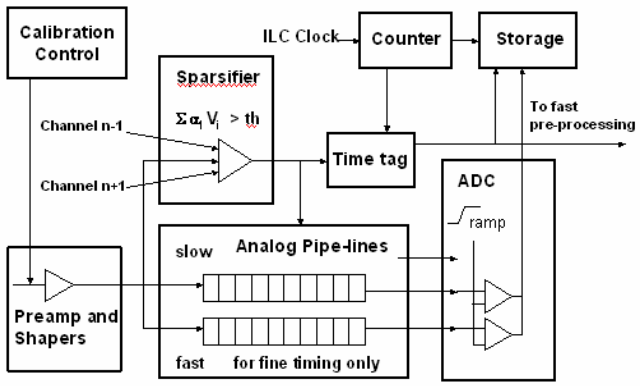

Figure 5. Foreseen front-end chip architecture

To summarize, the goal as seen today is to integrate 512 to 1024 channels in 90nm CMOS including amplifiers with a 20-30mV/MIP voltage gain over 20-40 MIPs, two pulse shaping options: 500ns-1µs, and 20-50ns for fine timing, zero suppression, pulse sampling, event buffering, AD conversion, digital pre-processing, calibration and power switching.

A. 180nm Chip

A chip has been submitted in 180nm CMOS technology, and tested in 2005. Each channel comprises a preamplifier-shaper, a sample and hold, and a comparator. The 180 nm CMOS technology and tools from United Microelectronics Corporation, Taiwan, were accessed through Europractice at IMEC (Leuven Belgium). The process allows six metal layers, various threshold voltages transistor options with thin oxide C_{ox} at 4.9 mF/m^2, 3.3V transistors, Metal Insulator Metal planar capacitors at 1 fF/µm^2.

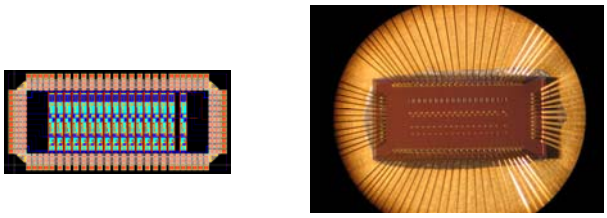

Figure 6. 180nm chip layout and picture.

The preamplifier is a buffered folded cascode structure providing a gain of 8 mV/ MIP, the shaper is an active CR-RC filter using an optimised version of the preamplifier. Power is 210 mW for the preamplifier and shaper. The chip has been extensively tested, process spreads within a wafer have been measured of the order of 3 % (Figure 7)

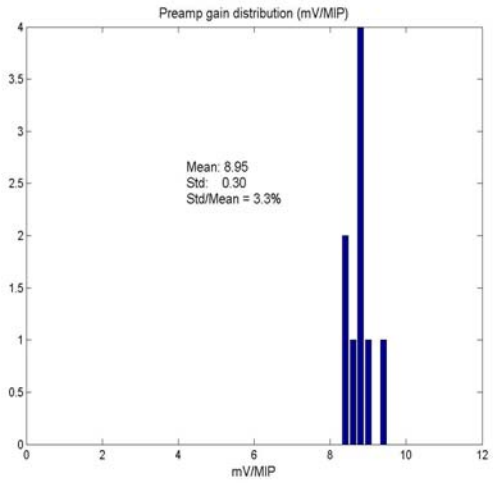

Figure 7. Process spreads (preamplifier gain) across a 180 nm CMOS wafer from UMC.

The shaper output noise is shown Figure 8. A total noise of 375 electrons + 10.4 be-/pF is found against 275 + 8.9 predicted by simulations, explained by a small instability of the shaper understood and fixed in the 130nm next version.

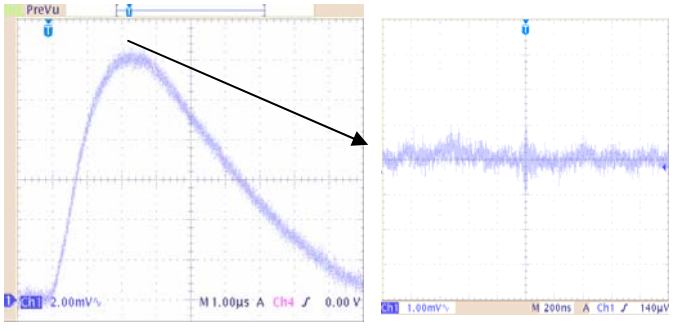

Figure 8. Shaper output. 375 electrons rms noise

As a conclusion, this process appeared to be stable and mature, models being accurate, only one failure found over twelve chips measured. As the 130 nm CMOS process from UMC was available beginning 2005, it was decided to switch the next design to this technology.

B. 130nm Chip

The motivations to go to thinner process were the following: chips are smaller, faster, more radiation tolerant, dissipate less power. In addition, support will be given in the next years to this technology that will be dominant in the industry.

However, some features make designs more constraining such as a reduced voltage swing (to keep the same electric field in the devices), leaks appear under the threshold voltage, as well as tunnel currents across the gates. Models are more complex, somewhat inaccurate in some cases as found later on.

Table 1 compares 180 and 130nm technologies.

Table 1.

	180nm	**130nm**
3.3V transistors	yes	yes
Logic power supply	1.8V	1.2V
Metal layers	6 Aluminum	8 Copper
MIM capacitors	1fF/µm^2	1.5fF/µm^2
Transistors	Three Vt options	+ Low leakage option

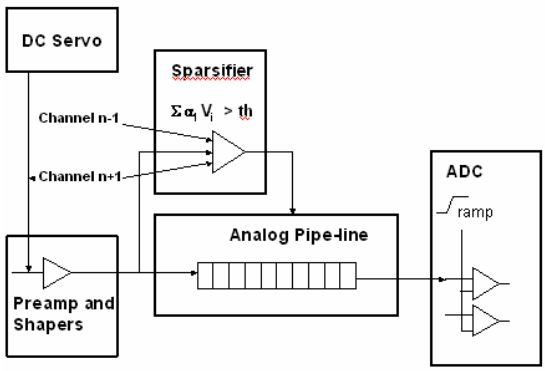

Figure 9. 130nm prototype chips architecture

The chip submitted in May 2005 was received in August and is being tested at the time of this workshop. Figure 10 shows a simulation of the analogue pipe-line signals and controls. Figure 11 shows layout and picture as well as analog sections in 180 and 130nm at the same scale.

A second chip in 130nm has been sent recently including the DC servo as shown in Figure 9, and an improved version of the sampler.

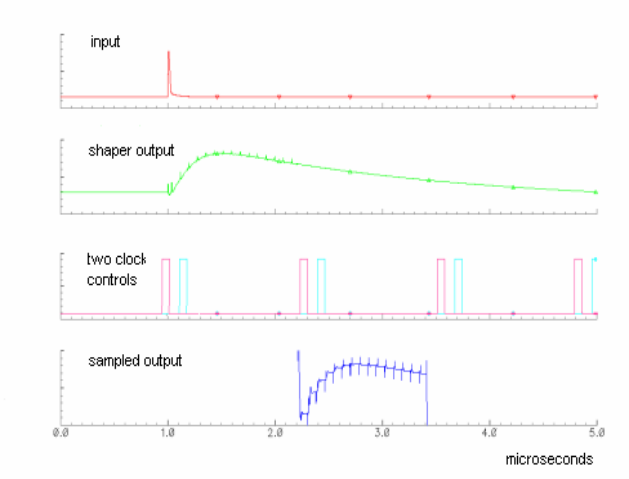

Figure 10 . Simulation of the analogue pipe-line signals and controls.

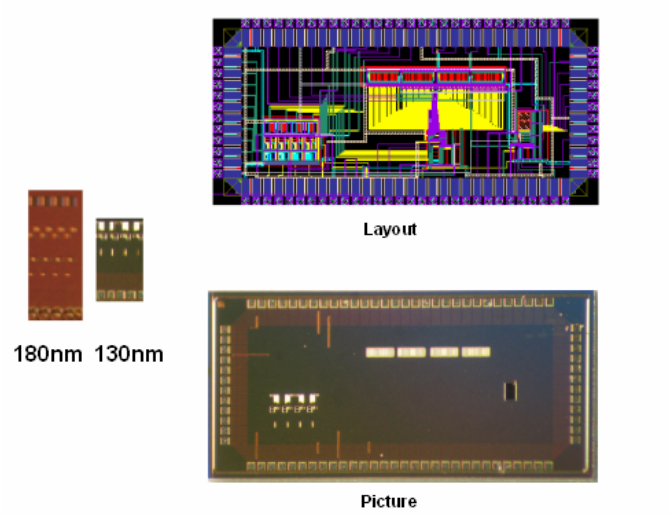

Figure 11. 130nm Silicon. Layout and picture.

During the design of these chips, NMOS noise was found much higher in simulations compared to the 180 nm process under the same sizes and transconductance conditions, and low Vt transistors somewhat leaky, as the low leakage option was not used. These features will be measured when the chips will be delivered. Verifications were done using Mentor rather than Cadence .

IV. Future Plans

If these 130 nm chips give the expected results and noise is within acceptable levels, next versions will include the fast shapers and samplers, as well as calibration and power cycling. A 128 channels chip able to read a Silicon detector is envisaged. Digital has to include chip control, buffer memory, processing for calibrations, amplitude and time estimations, raw data lossless compression. Digital library are available at Virtual Silicon Technologies, synthesis, place and route tools from Cadence together with the design kits provided by Europractice. Some IPs (PLLs, SRAM) are even available.

V. Conclusion

At the time this workshop takes place, a 180nm chip has been successfully designed and tested. This technology allows clearly to design the low noise mixed designs required by Silicon strips detectors. Two 130nm CMOS prototypes have been submitted including a full readout chain up to the AD conversion. Depending on the results, this work will be carried on with multi channel versions, the goal being to provide in 2007 chips able to read a full Silicon detector, including calibration and power cycling.

Acknowledgments

The authors are indebted to Erwin Deumens and Paul Malisse at IMEC for the efficient help provided along the chip designs, in particular at the verifications stage. Interface with UMC (Taiwan) was also extremely positive, thanks to their efforts.

References

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[2] R. Yarema. 3D Circuits Integration for High Energy Physics. These proceedings.